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PTO/SB/21 (09-04)

Approved for use through 07/31/2006. OMB 0651-0031

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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/065,589	
	Filing Date	Oct 31, 2002	
	First Named Inventor	Paterson, Allan	
	Art Unit	1763	
	Examiner Name	Goudreau, George	
Total Number of Pages in This Submission	8	Attorney Docket Number	2969.004

ENCLOSURES (Check all that apply)		
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Remarks Request for Certificate of Correction (5 pages) Certificate of Correction PTO/SB/44 in duplicate (2 pages) Return Receipt Postcard		

Certificate

SEP 15 2005

of Correction

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	SINSHEIMER, SCHIEBELHUT & BAGGETT		
Signature			
Printed name	Thomas F. Lebens		
Date	9/9/05	Reg. No.	38221

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This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 10/065,589
Applicant(s) : Paterson, et al.
Filed : 10/31/2002
TC/A.U. : 1763
Examiner : Goudreau, George

Docket No. : 2969.004
Customer No. : 26375
Confirmation No. : 9771

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Thomas F. Lebens
Registration No. 38,221
Attorney for Applicant(s)

**REQUEST FOR CERTIFICATE OF CORRECTION
PURSUANT TO 37 C.F.R. § 1.322**

Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Transmitted herewith is a Certificate of Correction for United States Patent 6,921,719 issued July 26, 2005. Upon reviewing the patent, the following errors were noted and should be corrected as follows:

In the CLAIMS:

Claim 1, column 12, line 60, delete "a" and insert --at--.

Claim 17, column 14, line 8, delete "wing" and insert --using--.

Claim 24, column 14, line 31, delete "wit" and insert --with--.

Claim 24, column 14, line 48, delete "water" and insert --wafer--.

The Certificate of Correction sets forth these corrections.

Remarks

A review of these documents confirms that the errors were made in the printing of the patent. Please see Exhibit "A", pages 2, 5 and 6 of Amendment A filed with the United States Patent and Trademark Office on October 4, 2004.

Since these errors for which a Certificate of Correction is requested are a result of the United States Patent and Trademark Office mistake, no fee is due (35 U.S.C. § 254). Please charge any deficiency or overpayment in fees to Deposit Account 50-1616.

Respectfully submitted,

SINSHEIMER, SCHIEBELHUT & BAGGETT

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Reg. No. 38,221

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SEP 19 2005



Amendments To The Claims

Claim 1 (currently amended): A method of preparing a whole wafer of semiconductor material, having opposed front and back sides with respective surfaces and having at least one electronic device, comprising the steps of:

covering the frontside of the wafer with a whole wafer frontside substrate;
supporting the whole wafer with a whole wafer support coupled to the whole wafer frontside substrate, with the whole wafer frontside substrate protecting said at least one electronic device;

said whole wafer including a whole wafer substrate having an initial thickness and which includes said whole wafer backside;

thinning the whole wafer substrate, reducing its thickness to expose a new whole wafer backside surface at the backside of the whole wafer; [[and]]

strengthening and rigidifying at least a portion of the new whole wafer backside surface to strengthen and rigidify at least a portion of the whole wafer; and

removing the whole wafer frontside substrate, exposing said at least one electronic device while maintaining the strengthening and rigidifying of at least the portion of the new whole wafer backside surface ~~the attachment of the whole wafer backside substrate to the whole wafer backside surface to strengthen and rigidify~~ at least the portion of the whole wafer.

Claim 2 (currently amended): The method of claim 1 ~~further comprising;~~
wherein the strengthening and rigidifying at least the portion of the new whole wafer backside surface comprises:

providing a whole wafer backside substrate; and

attaching the whole wafer backside substrate to at least [[a]] the portion of the new whole wafer backside surface to strengthen and rigidify the whole wafer.

Claim 17 (original): The method of claim 1 wherein said thinning step comprises etching the backside of said whole wafer using focused ion-beam etching techniques.

Claim 18 (original): The method of claim 1 wherein the step of covering the frontside of the wafer with a whole wafer frontside substrate comprises attaching the whole wafer frontside substrate to the frontside of the wafer with an adhesive.

Claim 19 (original): The method of claim 18 further comprising the step of cleaning the frontside of the wafer after removing the whole wafer frontside substrate.

Claim 20 (currently amended): The method of claim 2 wherein the new whole wafer backside surface has a ~~preselected~~-size and the whole wafer backside substrate is sized with a smaller size and the step of attaching comprises attaching the whole wafer backside substrate to a ~~preselected~~-portion of said new whole wafer backside surface.

Claim 21 (original): The method of claim 1 wherein said whole wafer frontside substrate is substantially rigid.

Claim 22 (original): The method of claim 1 wherein said whole wafer frontside substrate is substantially flexible.

Claim 23 (original): The method of claim 1 wherein said whole wafer frontside substrate is vacuum-porous.

Claim 24 (original): A method of preparing a whole semiconductor wafer having opposed front and back sides with respective surfaces and having at least one electronic device, comprising the steps of:

covering the frontside of the wafer with a whole wafer frontside substrate;

supporting the whole wafer frontside substrate in a vacuum chuck, with the whole wafer frontside substrate protecting said at least one electronic device;

said whole wafer including a whole wafer substrate having an initial thickness and which includes said whole wafer backside;

thinning the whole wafer substrate, reducing its thickness by grinding the wafer substrate to expose a ground surface at the backside of the whole wafer;

polishing the backside of the whole wafer to provide a new whole wafer backside substrate surface;

attaching the whole wafer backside substrate to the new whole wafer backside surface to strengthen and rigidify the whole wafer; and

removing the whole wafer frontside substrate, exposing said at least one electronic device while maintaining the attachment of the whole wafer backside substrate to the whole wafer backside surface to strengthen and rigidify the whole wafer.

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 6,921,719
DATED : July 26, 2005
INVENTOR(S) : Paterson, et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent
is hereby corrected as shown below:

In the CLAIMS:

Claim 1, column 12, line 60, delete "a" and insert --at--.

Claim 17, column 14, line 8, delete "wing" and insert --using--.

Claim 24, column 14, line 31, delete "wit" and insert --with--.

Claim 24, column 14, line 48, delete "water" and insert --wafer--.

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PATENT NO: 6,921,719

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This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application for to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.